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(54) MOS TRANSISTOR STRUCTURE AND CHARGE TRANSFER DEVICE WITH IT

(57)Abstract:

PURPOSE: To provide a MOS transistor structure that realize a lower drain voltage without decrease of conversion ratio of output voltage to input voltage and decrease of margin of the output voltage.

CONSTITUTION: An enhancement MOS transistor (A) is structured by forming a P type well region 14 that comprises a substrate with a two-layer structure of upper and lower layers, forming two N++ type impurity regions 15 and 16 on a substrate surface side of P+ type impurity region 14b of the upper layer of two layer structured P-type well region 14 and arranging a gate electrode 18 at the upper part of a channel region between these regions 15 and 16. A depletion type MOS transistor (B) is structured by forming 2 N++ type impurity region 19 and 20 on the substrate surface side of P+ type impurity region 14b, forming N+ type impurity region 21 on the substrate surface side of

channel region between these regions 15 and 16 and arranging a gate electrode 22 on it.

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CLAIMS

[Claim(s)]

[Claim 1] It is the MOS transistor structure where the enhancement type MOS transistor and the depletion type MOS transistor were formed on the same substrate. Said substrate consists of a P type substrate of vertical two-layer structure. Said enhancement type MOS transistor Two N type impurity ranges formed in the front-face side of the upper layer of the P type substrate of said two-layer structure, It consists of a gate electrode arranged above the channel field between this two N type impurity range. Said depletion type MOS transistor Two N type impurity ranges formed in the front-face side of the upper layer of the P type substrate of said two-layer structure, MOS transistor structure characterized by consisting of an N type impurity range formed in the front-face side of the channel field between this two N type impurity layer, and a gate electrode arranged above this N type impurity range.

[Claim 2] The P type substrate of said two-layer structure is MOS transistor structure according to claim 1 characterized by setting up the high impurity concentration of the upper layer more deeply than lower layer high impurity concentration.

[Claim 3] The P type substrate of said two-layer structure is MOS transistor structure according to claim 1 characterized by setting up the high impurity concentration of the upper layer more thinly than lower layer high impurity concentration.

[Claim 4] The charge transfer equipment which is charge transfer equipment equipped with the charge transfer section which transmits a signal charge, the charge detecting element which detects the signal charge transmitted by this charge transfer section, and the output section which changes and outputs the signal charge detected by this charge detecting element to an electrical signal, and is characterized by to be constituted said output section using MOS transistor structure according to claim 1, 2, or 3.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the charge transfer equipment which constituted the output section using the MOS transistor structure where the enhancement type MOS transistor and the depletion type MOS transistor were especially formed on the same substrate, and this about the charge transfer equipment which used MOS transistor structure and this.

[0002]

[Description of the Prior Art] The MOS transistor circuit which consists of combination of an enhancement type MOS transistor and a depletion type MOS transistor is used as an example as a source follower circuit which constitutes the output section of a solid state camera. Here, an enhancement type MOS transistor is an MOS transistor of the type with which a drain current flows for the first time when gate voltage is applied more than threshold voltage, and even if a depletion type MOS transistor does not apply an electrical potential difference to the gate, it is an MOS transistor of the type with which a drain current flows.

[0003] When manufacturing this enhancement type MOS transistor and a depletion type MOS transistor, the MOS transistor structure which formed the transistor of both types on the same substrate from the aim which communalizes a production process and plans cost reduction is common. Moreover, in this MOS transistor structure, the P type substrate which forms an enhancement type MOS transistor and a depletion type MOS transistor was formed by the monolayer.

[0004]

[Problem(s) to be Solved by the Invention] By the way, in the solid state camera, in order to raise commodity value, low-battery-ization of a drain electrical potential difference with the highest electrical potential difference is attained in the output section. However, with the conventional MOS transistor structure in which the enhancement type MOS transistor and the depletion type MOS transistor were formed on the same substrate, if low-battery-ization of a drain electrical potential difference is attained, since the potential under the gate also becomes shallow, especially in an enhancement type MOS transistor, accumulation-ization of a hole will arise from gate voltage turning

into a low battery.

[0005] Accumulation means the phenomenon in which many majority carriers gather for the semi-conductor interface which touches an oxide film, in metal-oxide-semiconductor structure here. Therefore, with the conventional MOS transistor structure, when low-battery-ization of a drain electrical potential difference was attained, there was a problem that the conversion rate (gain) of output voltage to input voltage fell sharply. Moreover, the margin of the output voltage by power-source variation, potential variation, etc. of a drain electrical potential difference was lost, and there was also a problem of it becoming impossible to guarantee the stable output voltage.

[0006] This invention is made in view of the above-mentioned technical problem, and the place made into the purpose is to offer the MOS transistor structure which enabled low-battery-ization of a drain electrical potential difference, without reducing the conversion rate of output voltage to input voltage, or losing the margin of output voltage.

[0007]

[Means for Solving the Problem] A substrate consists of a P type substrate of vertical two-layer structure with the MOS transistor structure by this invention. While an enhancement type MOS transistor is constituted by the gate electrode arranged above the channel field between two N type impurity ranges formed in the front-face side of the upper layer of the P type substrate of this two-layer structure, and this two N type impurity range Two N type impurity ranges formed in the front-face side of the upper layer of the P type substrate of two-layer structure, The depletion type MOS transistor is constituted by the gate electrode arranged the N type impurity range formed in the front-face side of the channel field between this two N type impurity layer, and above this N type impurity range.

[0008]

[Function] In the MOS transistor structure of the above-mentioned configuration, when the high impurity concentration of the upper layer of two-layer structure was set up more deeply than lower layer it and a drain electrical potential difference is low-battery-ized, the potential under the gate does not change with upper operations by the enhancement type MOS transistor. Therefore, accumulation-ization of a hole can be prevented. On the other hand, in a depletion type MOS transistor, a double lump of the maximum potential when seting a substrate electrical potential difference constant and the minimum potential becomes easy according to two-layer-ized structure.

[0009]

[Example] Hereafter, the example of this invention is explained to a detail based on a

drawing. Drawing 6 is a block diagram with which this invention is applied and in which showing an example of the CCD mold solid state camera of the INTARAIN transmittal mode, for example. In drawing 6 , two-dimensional array is carried out, photo electric conversion of the incident light is carried out, and the image pick-up section 63 is constituted by the perpendicular transfer register 62 which transmits perpendicularly the signal charge which was allotted for every vertical file of two or more optoelectric transducers 61 which accumulate the signal charge obtained by this, and two or more of these optoelectric transducers 61, and was read from the optoelectric transducer 61.

[0010] In this image pick-up section 63, an optoelectric transducer 61 is constituted by the photodiode and the perpendicular transfer register 62 is constituted by CCD. The signal charge moved to the perpendicular transfer register 62 is transmitted to the level transfer register 64 in order of partial [equivalent to the 1 scanning line / every]. The signal charge for this 1 scanning line is horizontally transmitted one by one with the level transfer register 64. The charge detecting element 65 which detects the signal charge transmitted to the last edge of the level transfer register 64 and which consists of FDA (Floating DiffusionAmplifier), for example is allotted.

[0011] In this charge detecting element 65, the signal charge transmitted with the level transfer register 64 is transmitted to the floating diffusion FD through the output gate OG. The potential of this floating diffusion FD is reset by the reset drain electrical potential difference VRD with a predetermined period by reset pulse phiRG. The output section 66 which changes and outputs the signal charge transmitted to the floating diffusion FD of the charge detecting element 65 to an electrical potential difference is allotted to the latter part of the charge detecting element 65.

[0012] This output section 66 is constituted by two steps of source follower circuits which consist of MOS transistor Q1L and Q2L a driving-side MOS transistor Q1D, Q2D, and load side. And bias of each gate of MOS transistor Q1L and Q2L is carried out in common by DC power supply 67 the load side, and the gate of driving-side MOS transistor Q1D of the first rank is connected to the floating diffusion FD of the charge detecting element 65.

[0013] In this output section 66, driving-side MOS transistor Q1D of the first rank has enhancement type MOS transistor composition, and MOS transistor Q1L and Q2L have depletion type MOS transistor composition the driving-side MOS transistor Q2D [the 2nd step of], and load side. The example of this invention hereafter applied to the source follower circuit which constitutes the output section 66 of this CCD mold solid state camera is explained. In addition, the output section 66 is explained as what is

formed on the same substrate as the body of equipment of a CCD mold solid state camera.

[0014] Drawing 1 is the sectional view showing the 1st example of the MOS transistor structure by this invention, (A) shows the cross-section structure of an enhancement type MOS transistor, and (B) shows the cross-section structure of a depletion type MOS transistor, respectively. drawing 1 -- setting -- the same N type silicon substrate 11 top as the body of equipment -- the 1st P type -- a well -- a field 12 forms -- having -- further -- the N type impurity range 13 -- minding -- the 2nd P type -- a well -- the field 14 is formed as a P type substrate of the output section 66.

[0015] this 2nd P type -- a well -- a field 14 -- lower layer P type impurity range 14a and this lower layer P type impurity range 14a -- P+ of the upper layer with deep concentration It has two-layer structure which consists of mold impurity range 14b. this 2nd P type -- a well -- if in charge of forming a field 14 -- the 2nd P type -- a well -- a mask is used for the field which forms a field 14, and the ion implantation of the impurity ion of deep concentration is continuously carried out the ion implantation of the impurity ion of thin concentration with high energy and carried out to it by low energy using the same mask. thereby -- the 2nd P type -- a well ---izing of the field 14 can be carried out [two-layer] easily.

[0016] drawing 1 (A) -- setting -- the 2nd P type -- a well -- P+ of the upper layer of a field 14 Two N++ mold impurity ranges 15 and 16 used as a drain field and a source field are formed in the substrate front-face side of mold impurity range 14b. And the gate electrode 18 is arranged above two N++ mold impurity ranges 15 and the channel field between 16 through gate oxide 17. Thereby, the enhancement type MOS transistor is constituted.

[0017] drawing 1 (B) -- setting -- the 2nd P type -- a well -- P+ of the upper layer of a field 14 two N++ mold impurity ranges 19 and 20 used as a drain field and a source field form in the substrate front-face side of mold impurity range 14b -- having -- further -- the substrate front-face side of these two N++ mold impurity ranges 15 and the channel field between 16 -- N+ The mold impurity range 21 is formed. And N+ The gate electrode 22 is arranged above the mold impurity range 21 through gate oxide 17. Thereby, the depletion type MOS transistor is constituted.

[0018] the 2nd P type which is a P type substrate in the conventional MOS transistor structure here when the conventional example is considered -- a well -- the field 14 was monolayer structure. For this reason, drain electrical potential difference VD When it low-battery-izes, it is gate voltage VG. Although it became a low battery, since the potential under the gate also became shallow as a broken line showed to drawing 3 (A),

there was a problem which accumulation-ization of a hole produces by the conventional enhancement type MOS transistor. In addition, the continuous line shows the potential before low-battery-izing.

[0019] on the other hand -- a depletion type MOS transistor -- an enhancement type MOS transistor and these conditions -- the 2nd P type – a well -- since the double lump of the maximum potential when seting a substrate electrical potential difference constant and the potential of the minimum potential is difficult by forming the field 14 as shown in drawing 3 (B), the punch-through produced in the drain current which becomes dominant at a depletion type MOS transistor and the N type silicon substrate 11 - gate inter-electrode poses a problem.

[0020] on the other hand, with the MOS transistor structure by the 1st example of the above-mentioned configuration the 2nd P type -- a well -- P+ with the substrate front-face side of a field 14 deep [concentration] By being mold impurity range 14b It sets to an enhancement type MOS transistor (A), and is the drain electrical potential difference VD. It low-battery-izes and is gate voltage VG. Since the potential under the gate does not change as a broken line shows to drawing 2 (A) even if it becomes a low battery the 2nd P type -- a well -- accumulation-ization of the hole of a field 14 can be prevented.

[0021] Thereby, it is the drain electrical potential difference VD. Even if it low-battery-izes, the conversion rate of output voltage to input voltage does not fall sharply, or the margin of output voltage is not lost by power-source variation, potential variation, etc. of a drain electrical potential difference. on the other hand -- a depletion type MOS transistor (B) -- the 2nd P type -- a well -- since a double lump of the maximum potential and the minimum potential becomes easy as by having made the field 14 into two-layer structure shows to drawing 2 (B), the punch-through produced between the N type silicon substrate 11 - the gate electrode 22 can be prevented.

[0022] Drawing 4 is the sectional view showing the 2nd example of the MOS transistor structure by this invention, (A) shows the cross-section structure of an enhancement type MOS transistor, and (B) shows the cross-section structure of a depletion type MOS transistor, respectively. In addition, among drawing, the same sign is given to drawing 1 and an equivalent part, and it is shown. drawing 4 -- setting -- the same N type silicon substrate 11 top as the body of equipment -- the 1st P type -- a well -- a field 12 forms -- having -- further -- the N type impurity range 13 -- minding -- the 2nd P type -- a well -- the field 24 of the point currently formed as a P type substrate of the output section 66 shown in drawing 6 is the same as that of the case of the 1st example.

[0023] this 2nd P type -- a well -- a field 24 -- lower layer P+ It has two-layer structure

which consists of P type impurity range 24b of the upper layer with thin concentration from mold impurity range 24a and this lower layer P type impurity range 24a. this 2nd P type -- a well -- if in charge of forming a field 24 -- the 2nd P type -- a well -- a mask is used for the field which forms a field 24, and the ion implantation of the impurity ion of thin concentration is continuously carried out the ion implantation of the impurity ion of deep concentration with high energy and carried out to it by low energy using the same mask. thereby -- the 2nd P type -- a well ---izing of the field 24 can be carried out [two-layer] easily.

[0024] drawing 4 (A) -- setting -- the 2nd P type -- a well -- two N++ mold impurity ranges 15 and 16 used as a drain field and a source field are formed in the substrate front-face side of P type impurity range 24b of the upper layer of a field 24. And the gate electrode 18 is arranged above two N++ mold impurity ranges 15 and the channel field between 16 through gate oxide 17. Thereby, the enhancement type MOS transistor is constituted.

[0025] drawing 4 (B) -- setting -- the 2nd P type -- a well -- two N++ mold impurity ranges 19 and 20 used as a drain field and a source field form in the substrate front-face side of P type impurity range 24b of the upper layer of a field 24 -- having -- further -- the substrate front-face side of these two N++ mold impurity ranges 15 and the channel field between 16 -- N+ The mold impurity range 21 is formed. And N+ The gate electrode 22 is arranged above the mold impurity range 21 through gate oxide 17. Thereby, the depletion type MOS transistor is constituted.

[0026] In the MOS transistor structure by the 2nd example of the above-mentioned configuration the 2nd P type -- a well -- a field 24 -- two-layer ---izing -- P+ with deep concentration When mold impurity range 24a formed, in an enhancement type MOS transistor (A) Since the potential under the gate becomes shallow and there is sufficient margin to accumulation-izing of a hole as a continuous line shows to drawing 5 (A), it is the drain electrical potential difference VD. Even if it low-battery-izes, as a broken line shows to this drawing, accumulation-ization of a hole does not arise.

[0027] on the other hand -- a depletion type MOS transistor (B) -- the 2nd P type -- a well -- a field 24 -- two-layer ---izing -- the deep location under the gate -- P+ with concentration higher than the upper layer the case where a substrate electrical potential difference is set as the same electrical potential difference as the former by having formed mold impurity range 24a -- P+ The potential of mold impurity range 24a becomes shallower than before. When this low-battery-izes a drain electrical potential difference, <A HREF="/Tokujitu/tjitemdrw.ipdl?N0000=239&N0500=1E_N/;?8=68=6:///&N0001=614&N0552=9&N 0553= 000007" TARGET="tjitemdrw">

drawing 5 Since the potential under the gate becomes shallower as a broken line shows to (B), the problem of the punch-through produced between the N type silicon substrate 11 - the gate electrode 22 is improvable.

[0028] In addition, in the above-mentioned example, although the case where the MOS transistor structure by this invention was applied to the output section in the so-called CCD area sensor to which two-dimensional array of the optoelectric transducer was carried out was explained, an optoelectric transducer can apply also like the output section in the so-called CCD line sensor arranged by the single tier, and the output section in a CCD mold delay element.

[0029] Furthermore, this invention is not limited to application in the output section in charge transfer equipment, and can be applied to the MOS transistor structure complete by which the enhancement type MOS transistor and the depletion type MOS transistor were formed on the same substrate.

[0030]

[Effect of the Invention] In the MOS transistor structure where the enhancement type MOS transistor and the depletion type MOS transistor were formed on the same P type substrate according to this invention as explained above By making a P type substrate into vertical two-layer structure, for example, setting up the upper high impurity concentration more deeply than lower layer it When a drain electrical potential difference is low-battery-ized, in an enhancement type MOS transistor Since the potential under the gate does not change, accumulation-ization of a hole can be prevented. In a depletion type MOS transistor Since a double lump of the maximum potential when seting a substrate electrical potential difference constant and the minimum potential becomes easy, the punch-through produced between a substrate - the gate can be prevented.

[0031] Thus, when a drain electrical potential difference is low-battery-ized, low-battery-ization of a drain electrical potential difference is attained by the ability preventing accumulation-ization of the hole where gate voltage especially also turns into a low battery, and poses a problem by the enhancement type MOS transistor, without reducing the conversion rate of output voltage to input voltage, or losing the margin of output voltage.

[0032] Moreover, since low-battery-ization of a drain electrical potential difference is attained without reducing the conversion rate of output voltage to input voltage by constituting the output section of charge transfer equipments, such as the charge transfer section and a delay element, in a solid state camera using the MOS transistor structure by this invention, or losing the margin of output voltage, it also becomes being able to

raise commodity value, such as a solid state camera and a delay element, by low-battery-ization of the highest drain electrical potential difference in the output section.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view showing the 1st example of this invention.

[Drawing 2] It is a potential Fig. concerning the 1st example.

[Drawing 3] It is a potential Fig. concerning the conventional example.

[Drawing 4] It is the sectional view showing the 2nd example of this invention.

[Drawing 5] It is a potential Fig. concerning the 2nd example.

[Drawing 6] It is the block diagram of an example of a CCD mold solid state camera.

[Description of Notations]

11 N Type Silicon Substrate

12 The 1st is Field P Well.

14 24 The 2nd is a field (P type substrate) P well.

15, 16, 19, 20 N++ mold impurity range

21 N+ Mold Impurity Range

18 22 Gate electrode